

## CLAIMS

- 1 1. A phase-locked-loop (PLL) comprising:  
2 an oscillator responsive to a control signal by producing a PLL output signal, a  
3 phase comparator responsive to a PLL input signal and the PLL output signal by  
4 detecting the phase difference between the two signals and producing a control  
5 signal indicative of that difference, the control signal being coupled to the  
6 oscillator, and control circuitry responsive to deviations of the PLL input signal's  
7 frequency outside a predetermined input frequency range by forcing the  
8 frequency of the PLL output to a predetermined value.
- 1 2. The PLL of claim 1 wherein the control circuit includes beat frequency circuitry that  
2 detects deviations of the input frequency outside the predetermined input frequency  
3 range.
- 1 3. The PLL of claim 1 wherein the control circuit includes voltage measurement  
2 circuitry which determines whether the PLL input signal's frequency deviates  
3 outside the predetermined input frequency range by measuring the voltage of  
4 said control signal coupled to the oscillator.
- 1 4. The PLL of claim 1 wherein said control signal from the phase comparator is an  
2 analog signal.
- 1 5. The PLL of claim 4 wherein said control signal is coupled to said oscillator  
2 through an analog to digital converter (ADC) and a digital to analog converter  
3 (DAC), and the control circuit determines frequency deviations outside the  
4 predetermined input frequency range by comparing the digital signal to digital  
5 values representative of the limits of the predetermined input frequency range.

- 1 6. The PLL of claim 1 wherein the predetermined frequency to which the output  
2 signal is forced falls within the predetermined input frequency range.
- 1 7. The PLL of claim 6 wherein the control circuit monitors the input signal's  
2 frequency and allows the PLL to lock onto the input signal should the input signal  
3 frequency return to the range of predetermined input frequencies.
- 1 8. The PLL of claim 7 wherein the control circuit suppresses out of range frequency  
2 indications for a predetermined time period to allow the PLL to lock onto an input  
3 signal whose frequency has returned to within a predetermined range of input  
4 frequencies.
- 1 9. An apparatus for providing a synchronized clock signal, comprising:  
2 a clock source that produces a clock output signal,  
3 a PLL responsive to the clock output signal, said PLL comprising:  
4 an oscillator responsive to a control signal by producing a PLL output signal,  
5 a phase comparator responsive to the clock signal and to the PLL output signal  
6 by detecting the phase difference between the two signals and producing a  
7 control signal indicative of that difference, the control signal being coupled to the  
8 oscillator, and control circuitry responsive to deviations of the clock signal's  
9 frequency outside a predetermined input frequency range by forcing the  
10 frequency of the PLL output to a predetermined value.
- 1 10. The apparatus of claim 9 wherein the control circuit includes a beat frequency  
2 detector that is responsive to deviations of the clock frequency outside the  
3 predetermined input frequency range.

1 11. The apparatus of claim 9 wherein the control circuit includes voltage  
2 measurement circuitry that determines whether the clock signal's frequency  
3 deviates outside the predetermined input frequency range by measuring the  
4 voltage of said control signal coupled to the oscillator.

1     12.     The apparatus of claim 9 wherein said control signal from the phase comparator  
2     is an analog signal.

1 13. The apparatus of claim 12 wherein said control signal is coupled to said oscillator  
2 through an analog to digital converter (ADC) and a digital to analog converter  
3 (DAC), and the control ~~circuit~~ determines frequency deviations outside the  
4 predetermined input frequency range by comparing the digital signal to digital  
5 values representative of the limits of the predetermined input frequency range.

1 14. The apparatus of claim 9 wherein the predetermined frequency to which the  
2 output signal is forced falls within the predetermined input frequency range.

1     15.     The apparatus of claim 14 wherein the control circuit monitors the input signal's  
2           frequency and allows the PLL to lock onto the input signal should the input signal  
3           frequency return to a frequency within the predetermined input frequency range.

1     16.     The apparatus of claim 15 wherein the control circuit suppresses out of range  
2     frequency indications for a predetermined time period to allow the PLL to lock  
3     onto a clock signal whose frequency has returned to within a predetermined  
4     range of input frequencies.

1 17. The apparatus of claim 16 further comprising:  
2 ~~a plurality of clock signal inputs, and~~



6 (b) controlling the frequency of an output signal from an oscillator with said control  
 7 signal such that the output signal from the oscillator is proportional in frequency to  
 8 the input signal,  
 9 (c) detecting deviations of the input signal's frequency outside a predetermined  
 10 input frequency range, and  
 11 (d) forcing the frequency of the oscillator output signal to a predetermined value  
 12 when a deviation of the input signal's frequency outside a predetermined range is  
 13 detected.

1 21. The method of claim 20 wherein step (d) comprises:  
 2 (c1) the step of measuring a beat frequency between the input and output signals.

1 22. The method of claim 20 wherein step (c) comprises:  
 2 (c2) the step of measuring the voltage of said control signal coupled to the oscillator.

1 23. The method of claim 22 wherein step (c2) comprises the steps of:  
 2 (c3) converting the control signal from an analog signal to a digital signal  
 3 (c4) comparing the digital signal to digital values representative of the limits of  
 4 the predetermined input frequency range.

1 24. The method of claim 23 further comprising the step of:  
 2 (e) allowing the frequency of the output signal to return to a value that is  
 3 proportional to the phase difference between the input and output signals if the  
 4 input signal frequency returns to the range of predetermined input frequencies.

1 25. The method of claim 24 further comprising the step of:  
 2 (f) suppressing out of range frequency indications for a predetermined time  
 3 period to allow the oscillator output signal to return to a frequency that is

- 4 proportional to that of an input signal <sup>21</sup> whose frequency has returned to a value  
5 ~~within the range of predetermined input frequencies.~~

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